



BUR920010102US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Fried et al.
Serial No.: 10/675,625
Filing Date: September 30, 2003
Title: FinFET CMOS with NVRAM Capability

Examiner:
Group Art Unit: 2812

Office of Initial Patent Examination's Filing Receipt Corrections
Assistant Commissioner of Patents
Washington, D.C. 20231


Request for Correction to Filing Receipt

Sir:

In response to the Filing Receipt dated 1/2/2004, Applicants hereby request that the Domestic priority data as claimed by applicant be corrected to 3/19/2002. A copy of the original filing receipt is attached.

Dated: 2/20/04

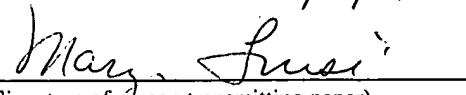
Respectfully submitted,
For: Fried et al.

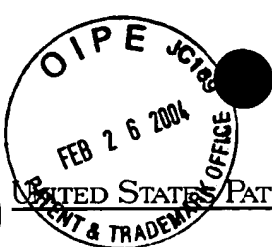
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CERTIFICATE OF MAILING UNDER 37 CFR 1.8

I certify that this correspondence is being transmitted by mail to the United States Patent and Trademark Office to: Office of Initial Patent Examination's Filing Receipt Corrections Art Unit 2812 on 2/20/04 by

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/675,625	09/30/2003	2812	0.00	BUR920010102US2	7	4	1

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CONFIRMATION NO. 6080

FILING RECEIPT



OC000000011597432

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Applicant(s)

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 Edward J. Nowak, Essex Junction, VT;

Domestic Priority data as claimed by applicant

This application is a DIV of 10/063,095 03/19/2002 PAT 6,657,252 *
 (*)Data provided by applicant is not consistent with PTO records.

Foreign Applications

If Required, Foreign Filing License Granted: 12/31/2003

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

FinFET CMOS with NVRAM capability

Preliminary Class

438

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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